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Patent Application

Applicant(s): D.E. Parson et al.
Case: 3-2-1-4
Serial No.: 09/583,057
Filing Date: May 30, 2000
Group: 2184
Examiner: Timothy M. Bonura

Title: Control Method and Apparatus for Testing of Multiple Processor Integrated Circuits and Other Digital Systems

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APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants hereby appeal the second rejection dated September 10, 2003 of claims 1-20 of the above-identified application.

REAL PARTY IN INTEREST

The present application is assigned to Agere Systems Inc. The assignee Agere Systems Inc. is the real party in interest.

RELATED APPEALS AND INTERFERENCES

There are no known related appeals and interferences.

STATUS OF CLAIMS

The present application was filed on May 30, 2000 with claims 1-20. Claims 1-20 remain pending. Claims 1, 13, 15, 19 and 20 are the independent claims.

Claims 1-20 stand twice rejected under 35 U.S.C. §103(a). Claims 1-20 are appealed.

STATUS OF AMENDMENTS

There have been no amendments filed subsequent to the final rejection.

SUMMARY OF INVENTION

The present invention is directed to methods and apparatus for testing a digital system comprising a plurality of processors. In accordance with the invention, at least a subset of the processors are defined as forming a group of processors to be subject to common control, and issuance of one or more commands for the group of processors is delayed until a group scan command is received for each of the processors in the group.

An illustrative embodiment of the invention is in the form of a multiple processor test system 100 as shown in FIG. 1. The system 100 includes processors X, Y and Z, a debugger 102, a scheduler 104, and a chain manager 106, as well as Test Access Port (TAP) managers 108X, 108Y and 108Z for the respective processors X, Y and Z. The operation of the system 100 is described as follows at page 5, line 21 to page 6, line 9:

> The operation of the system 100 will now be described for a given test configuration involving a designated group of the multiple processors. The debugger 102 via the scheduler 104 asks the chain manager 106 for a group identifier (GROUP ID) for a group of known size. A particular member of a group refers generally to one of the processors and its corresponding TAP manager. The chain manager 106 issues a GROUP ID and stores that GROUP ID as well as the size of the group. This GROUP ID is passed back to the debugger 102. Each of the TAP managers 108X, 108Y and 108Z includes a device-specific program for its corresponding processor, and issues one or more IEEE 1149.1 scan commands ending

with a group scan command which may be, e.g., an instruction register (IR) command and/or a data register (DR) command.

A group scan command in the illustrative embodiment refers generally to a final JTAG scan command that occurs before a desired synchronous or pseudo-synchronous behavior. The group scan command generated by one of the TAP managers in a group is delayed by the chain manager 106 until the TAP managers for all other group members issue a group scan command. The individual commands of the groups are then merged, and synchronously and simultaneously scanned into the scan chain 110 by the chain manager 106.

The chain manager 106 thus delays the issuance of the group scan commands for the members of the group until all members of the group arrive at an equivalent state in their control sequences.

FIG. 4 shows a timing diagram illustrating the delayed issuance of one or more commands for a group of processors until a group scan command is received for each of the processors in the group. As described at page 10, line 27 to page 11, line 14, debugger 102 issues a command to each of a group of TAP managers denoted TAP 0, TAP 1 and TAP N, corresponding to respective processors 0, 1 and N, using a single non-zero GROUP ID. Each TAP manager translates its debugger command into a sequence of JTAG commands, but the JTAG chain manager 106 delays issuing the final group scan JTAG commands onto the JTAG hardware scan chain 110 until the arrival of the final JTAG command for TAP N, i.e., the group scan command for TAP N. The JTAG chain manager then issues the JTAG group scan commands for processors 0, 1 and N on the scan chain as a single synchronous bit stream. As a result, initiation or termination of processor execution, or of any other processor operation controlled by JTAG commands, is synchronized or pseudo-synchronized for processors 0, 1 and N. The JTAG chain manager 106 thus defers transmission of the JTAG command bit stream onto the JTAG hardware scan chain until the arrival of the final JTAG command for a group of processors with a shared GROUP ID.

The present invention in the above-described illustrative embodiments provides a number of significant advantages over conventional approaches. For example, the claimed arrangements allow multiple processors to perform synchronous or pseudo-synchronous operations without requiring excessive coupling between individual processor debug systems as in conventional approaches. In addition, the processor grouping can be altered dynamically to allow for multiple groups of processors on the same scan chain and the alterations of these groups during a single debugging session. This control mechanism of the present invention is thus reusable for different numbers and arrangements of processors. See the specification at, for example, page 4, lines 9-16 and page 11, lines 16-21.

ISSUES PRESENTED FOR REVIEW

1. Whether claims 1, 10, 11, 13, 14, 19 and 20 are unpatentable under 35 U.S.C. §103(a) over U.S. Patent No. 5,253,359 (hereinafter "Spix") in view of U.S. Patent No. 6,028,983 (hereinafter "Jaber").

2. Whether claims 2 and 3 are unpatentable under §103(a) over Spix, Jaber and U.S. Patent No. 6,108,699 (hereinafter "Moiin").

3. Whether claims 4, 5, 8, 12 and 15-18 are unpatentable under §103(a) over Spix, Jaber and U.S. Patent No. 6,263,373 (hereinafter "Cromer").

4. Whether claims 6 and 7 are unpatentable under §103(a) over Spix, Jaber, Moiin and Cromer.

5. Whether claim 9 is unpatentable over unspecified references.

GROUPING OF CLAIMS

With regard to Issue 1, claims 1, 10, 11, 13, 14, 19 and 20 stand or fall together.

With regard to Issue 2, claim 2 stands or falls alone, and claim 3 stands or falls alone.

With regard to Issue 3, claims 4, 5, 8, 12 and 15-18 stand or fall together.

With regard to Issue 4, claim 6 stands or falls alone, and claim 7 stands or falls alone.

With regard to Issue 5, claim 9 stands or falls alone.

ARGUMENT

Issue 1

A proper *prima facie* case of obviousness requires that the cited references when combined must "teach or suggest all the claim limitations," and that there be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the references or to modify the reference teachings. See Manual of Patent Examining Procedure (MPEP), Eighth Edition, August 2001, §706.02(j).

Applicants submit that the Examiner has failed to establish a proper *prima facie* case of obviousness in the §103(a) rejection of claims 1, 10, 11, 13, 14, 19 and 20, in that the Spix and Jaber references, even if assumed to be combinable, fail to teach or suggest all the claim limitations, and in that no cogent motivation has been identified for combining the references or modifying the reference teachings to reach the claimed invention. Further, even if it is assumed that a proper *prima facie* case has been established, there are particular teachings in one or more of the references which controvert the obviousness argument put forth by the Examiner.

Each of independent claims 1, 13, 19 and 20 involves testing a digital system comprising a plurality of processors, and includes limitations relating to defining at least a subset of the processors as forming a group of processors to be subject to common control and delaying issuance of one or more commands for the group until a group scan command is received for each of the processors in the group.

As noted above, the present invention as set forth in these claims provides a number of significant advantages over conventional approaches. For example, the claimed arrangements allow the multiple processors to perform synchronous or pseudo-synchronous operations without requiring excessive coupling between individual processor debug systems as in the conventional approaches. In addition, the processor grouping can be altered dynamically to allow for multiple groups of processors on the same scan chain and the alterations of these groups during a single debugging session. This control mechanism of the present invention is thus reusable for different numbers and arrangements of processors.

Applicants submit that the proposed combination of Spix and Jaber fails to teach or suggest at least the above-noted limitations of each of independent claims 1, 13, 19 and 20, and furthermore fails to provide the associated advantages of the claimed invention.

The Examiner in formulating the §103(a) rejection acknowledges that Spix "does not disclose the use of a group scan command," and thus fails to teach or suggest an arrangement in which the issuance of one or more commands for a group of processors subject to common control is inhibited or otherwise delayed until a group scan command is received for each of the processors in the group. See the September 10, 2003 Office Action at page 3, line 3. However, the Examiner argues that such an arrangement would be obvious in view of Spix and the teachings in Jaber at column 3, lines 54-56, and column 4, lines 6-7 and 16-22. Applicants respectfully disagree. The relied-upon teachings from Jaber provide as follows, with emphasis supplied:

> Another object is an improved test apparatus and method of operation which limits voltage swings in scan testing of high-performance microprocessor chips.
>
> . . .
>
> Another object is an improved JTAG port in scan testing of a microprocessor chip.
>
> These and other objects, features and advantages are achieved in a test apparatus for design verification of at least one microprocessor chip having a compatible Joint Task Action Group (JTAG) terminal. A plurality of computer functional units are contained in the chip for testing of design verification through the compatible JTAG terminal. A test input terminal included in the JTAG terminal receives a scan string, the string being coupled to each computer functional unit through a first multiplexer. The scan input string is divided into a series of dedicated scan strings, each dedicated scan string being supplied to a selected functional unit through the first multiplexer. Each functional unit includes start and stop scan clocks for entering the dedicated scan string into the functional unit for test purposes.

Applicants submit that these teachings not only fail to meet the claim limitation that calls for delaying the issuance of one or more commands for a group of processors subject to common control until a group scan command is received for each of the processors in the group, but in fact directly

teach away from it. More specifically, by teaching that each functional unit includes its own start and stop clocks for processing a corresponding dedicated scan string portion of an input scan string, Jaber teaches away from the particular claimed arrangement involving delaying the issuance of one or more commands for a group of processors. This is further apparent from the passage at column 4, lines 26-35 of Jaber, which provides as follows:

> The compatible JTAG terminal includes further means for controlling the scan clocks to select a targeted functional unit for testing purposes while the scan strings for non-targeted functional units remain in an inactive state. By limiting the functional units under test, the voltage swing in the chip is reduced for test purposes; scan time for testing is decreased; memory space allocation for storing test results is reduced and design verification is not delayed by the loss of access to functional units due to a break in the scan signal.

The cited portions of Jaber appear to relate to independent control of the functional units. The relied-upon teachings thus fail to disclose the claimed arrangement in which the issuance of one or more commands is delayed, for a group of processors subject to common control, until a group scan command is received for each of the processors in the group.

Applicants respectfully submit that neither Spix nor Jaber provides any teaching or suggestion whatsoever regarding the claimed group scan command. As mentioned previously herein, one possible example of such a group scan command in an illustrative embodiment of the present invention is described as follows at page 6, lines 1-9 of the specification:

> A group scan command in the illustrative embodiment refers generally to a final JTAG scan command that occurs before a desired synchronous or pseudo-synchronous behavior. The group scan command generated by one of the TAP managers in a group is delayed by the chain manager 106 until the TAP managers for all other group members issue a group scan command. The individual commands of the groups are then merged, and synchronously and simultaneously scanned into the scan chain 110 by the chain manager 106.

The chain manager 106 thus delays the issuance of the group scan commands for the members of the group until all members of the group arrive at an equivalent state in their control sequences.

As noted above, the Examiner acknowledges that Spix "does not disclose the use of a group scan command" as claimed. Moreover, based on a search conducted by the undersigned in an electronic version of the Jaber reference taken from the database at the USPTO web site, the phrases "group scan" or "group scan command" apparently do not appear anywhere in the text of the Jaber reference. It is difficult to imagine how one could reasonably argue that Spix and Jaber collectively meet the group scan command limitation in question when neither reference makes any mention whatsoever regarding a group scan or a group scan command.

Each of claims 1, 13, 19 and 20 thus includes one or more limitations which are not taught or suggested by the proposed combination of Spix and Jaber. The combined teachings of these references therefore fail to "teach or suggest all the claim limitations" as would be required by a proper §103(a) rejection.

Also, as indicated previously, the Examiner has failed to identify a cogent motivation for combining the references or for modifying the reference teachings to reach the claimed invention.

Applicants initially submit that Spix and Jaber are in fact non-analogous art relative to one another. Spix is in the field of "maintenance and control of computer systems" and more specifically relates to "an integrated system for controlling and maintaining a high-speed supercomputer and its peripheral devices using a number of maintenance control units" (Spix, column 1, lines 24-30). The Jaber reference, by contrast, is in the integrated circuit scan testing art (Jaber, column 1, lines 7-10). One looking for teachings regarding scan testing of circuits or systems would not be motivated, absent some explicit suggestion, to look toward the supercomputer maintenance and control art. This disparity in the technical fields of Spix and Jaber is indicative of a lack of motivation to combine the references.

As was described above, neither Spix nor Jaber teaches or suggests the limitation of claims 1, 13, 19 and 20 that calls for delaying the issuance of one or more commands for a group of processors subject to common control until a group scan command is received for each of the

processors in the group. However, the Examiner argues that it would be obvious to combine or modify the teachings of these references to meet the limitation in question. The statement of obviousness provided by the Examiner at page 3, lines 5-8 of the September 10, 2003 Office Action is as follows:

> It would have been obvious to one of ordinary skill in the art at the time of the invention to include means to combine the Jaber reference with the Spix reference. Spix discloses that it would be useful for setting and sensing capability in a highly parallel processing system.

Applicants submit that this is a conclusory statement of obviousness, and insufficient to support the proposed combination or modification of the reference teachings.

The Federal Circuit has stated that when patentability turns on the question of obviousness, the obviousness determination "must be based on objective evidence of record" and that "this precedent has been reinforced in myriad decisions, and cannot be dispensed with." In re Sang-Su Lee, 277 F.3d 1338, 1343 (Fed. Cir. 2002). Moreover, the Federal Circuit has stated that "conclusory statements" by an examiner fail to adequately address the factual question of motivation, which is material to patentability and cannot be resolved "on subjective belief and unknown authority." Id. at 1343-1344. There has been no showing in the present §103(a) rejection of objective evidence of record that would motivate one skilled in the art to combine Spix and Jaber or to modify the proposed combination of Spix and Jaber to produce the particular limitations in question. Instead, the Examiner points to column 3, lines 22-27 of Spix, which provides as follows:

> It is clear that there is a need for a control and maintenance architecture specifically designed for the needs of a highly parallel multiprocessor system. Specifically, there is a need for a maintenance subsystem allowing setting and sensing capability for all internal machine registers, the ability to set and sense machine states by management of massive amounts of information, independent control of processor power up sequences, processor clocks, processor machine states, and peripheral devices.

Although this passage may be a motivation for the specific invention described in Spix, it fails to provide the requisite motivation for the proposed combination of Spix with an integrated circuit scan testing reference such as Jaber.

The above-quoted statement of obviousness given by the Examiner in the September 10, 2003 Office Action is thus believed to be precisely the type of subjective, conclusory statement that the Federal Circuit has indicated provides insufficient support for an obviousness rejection. It appears, in view of the above-quoted conclusory statement of obviousness provided by the Examiner, that the Examiner in combining Spix and Jaber has simply undertaken a hindsight-based piecemeal reconstruction of the claimed invention based on the disclosure provided by Applicants. Such an approach is improper.

Further, even if it is assumed that a proper *prima facie* case has been established, there are particular teachings in one or more of the references which controvert the obviousness argument put forth by the Examiner. For example, the Jaber reference, in accordance with the previously-described teachings from column 4, lines 6-35 thereof, teaches to limit the functional units under test by controlling the scan clocks to select a targeted functional unit for testing purposes while the scan strings for non-targeted functional units remain in an inactive state. It is believed that this is a direct teaching away from the claimed invention, which calls for delaying the issuance of one or more commands for a group of processors subject to common control until a group scan command is received for each of the processors in the group. Such a teaching away constitutes evidence of non-obviousness.

Applicants therefore respectfully submit that independent claims 1, 13, 19 and 20 are allowable over Spix, Jaber and the other art of record.

Dependent claims 10, 11 and 14 are believed allowable for at least the reasons identified above with regard to their respective independent claims.

The §103(a) rejection of claims 1, 10, 11, 13, 14, 19 and 20 over Spix and Jaber is therefore believed to be improper, and should be withdrawn.

Issue 2

Dependent claims 2 and 3, which depend from independent claim 1, are believed allowable for at least the reasons identified above with regard to claim 1.

The arguments presented above with regard to independent claim 1 are realleged and incorporated herein by reference.

Dependent claims 2 and 3 are also believed to define separately patentable subject manner over the art of record, as described below.

With regard to dependent claim 2, this claim calls for defining a group of processors in a chain manager in response to a group request received from a debugger. The Examiner argues that this limitation is obvious in view of Spix, Jaber and Moiin. However, the collective teachings of the cited references fail to meet the particular language of the limitation in question. The Examiner more specifically points to the node petitioning described in column 2, lines 10-20 of Moiin. This node petitioning, in combination with the teachings from Spix and Jaber, fails to teach or suggest the claimed defining of a group of processors in a chain manager in response to a group request received from a debugger.

With regard to dependent claim 3, this claim calls for a chain manager that establishes a group identifier for the group, stores the group identifier and a size of the group, and returns the group identifier to the debugger. Again, the Examiner argues that this limitation is obvious in view of Spix, Jaber and Moiin, relying more specifically on the node petitioning teachings of column 2, lines 10-20 of Moiin, when the collective teachings of these references fail to meet the particular language of the limitation in question. The node petitioning of Moiin, in conjunction with the teachings from Spix and Jaber, fails to teach or suggest the claimed arrangement in which a chain manager establishes a group identifier for the group, stores the group identifier and a size of the group, and returns the group identifier to the debugger.

Issue 3

Independent claim 15 stands rejected under §103(a) as being unpatentable over Spix, Jaber and Cromer. Claim 15 includes limitations similar to those of claims 1, 13, 19 and 20, and is therefore believed allowable for at least the reasons previously identified with regard to Issue 1

above, said reasons being hereby realleged and incorporated herein by reference. The Cromer reference fails to supplement the fundamental deficiencies of the proposed combination of Spix and Jaber with regard to these limitations. The Spix, Jaber and Cromer references, even if assumed to be combinable, fail to teach or suggest all of the limitations of claim 15. The §103(a) rejection of independent claim 15 over Spix, Jaber and Cromer is therefore believed to be improper and should be withdrawn.

Dependent claims 4, 5, 8, 12 and 16-18 are believed allowable for at least the reasons identified above with regard to their respective independent claims. The rejection of these claims should therefore also be withdrawn.

Issue 4

Dependent claims 6 and 7, which depend from independent claim 1, are believed allowable for at least the reasons identified above with regard to claim 1.

The arguments presented above with regard to independent claim 1 are realleged and incorporated herein by reference.

Dependent claims 6 and 7 are also believed to define separately patentable subject manner over the art of record, as described below.

With regard to dependent claim 6, this claim specifies that each processor and its corresponding TAP manager may have membership in only one group at a given point in time. The Examiner argues that this limitation is obvious in view of Spix, Jaber, Moiin and Cromer. However, the collective teachings of the cited references fail to meet the particular language of the limitation in question. Moreover, the Examiner has failed to identify the requisite motivation for the proposed combination.

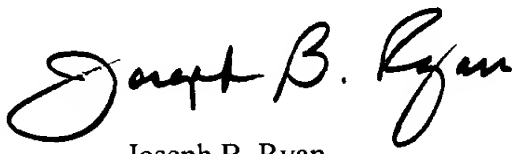
With regard to dependent claim 7, this claim specifies that each processor and its corresponding TAP manager may have membership in different groups of processors at different points in time. Again, the Examiner argues that this limitation is obvious in view of Spix, Jaber, Moiin and Cromer, when the collective teachings of these references fail to meet the particular language of the limitation in question. Moreover, the Examiner has failed to identify the requisite motivation for the proposed combination.

Issue 5

The Examiner has failed to provide any specific ground of rejection for dependent claim 9. The rejection of dependent claim 9 is therefore believed to be improper, and should be withdrawn. Dependent claim 9 should be indicated as containing allowable subject matter.

In view of the above, Applicants believe that claims 1-20 are in condition for allowance, and respectfully request withdrawal of the §103(a) rejections.

Respectfully submitted,



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APPENDIX

1. A method of testing a digital system comprising a plurality of processors, the method comprising the steps of:

defining at least a subset of the processors as forming a group of processors to be subject to common control; and

delaying issuance of one or more commands for the group until a group scan command is received for each of the processors in the group.

2. The method of claim 1 wherein the defining step includes defining the group of processors in a chain manager in response to a group request received from a debugger.

3. The method of claim 2 wherein the chain manager establishes a group identifier for the group, stores the group identifier and a size of the group, and returns the group identifier to the debugger.

4. The method of claim 1 wherein the commands comprise commands configured in accordance with the IEEE 1149.1 standard.

5. The method of claim 1 wherein the group scan commands for each of the processors in the group are generated by a Test Access Port (TAP) manager associated with the corresponding processor.

6. The method of claim 5 wherein each processor and its corresponding TAP manager is a member of only one group at a given point in time.

7. The method of claim 5 wherein each processor and its corresponding TAP manager is a member of different groups of processors at different points in time.

8. The method of claim 1 wherein the group of processors comprises a group of homogeneous processors.

9. The method of claim 8 wherein the delaying step provides synchronous control for the group of homogeneous processors.

10. The method of claim 1 wherein the group of processors comprises a group of heterogeneous processors.

11. The method of claim 10 wherein the delaying step provides pseudo-synchronous control for the group of heterogeneous processors.

12. The method of claim 1 wherein one or more of the group scan commands for each of the processors in the group of processors are supplied as a single serial bit stream to a hardware scan chain associated with the processors.

13. An apparatus for use in testing a digital system comprising a plurality of processors, the apparatus comprising:

a chain manager operative to define at least a subset of the processors as forming a group of processors to be subject to common control, and to delay issuance of one or more commands for the group until a group scan command is received for each of the processors in the group.

14. The apparatus of claim 13 wherein the chain manager is implemented at least in part in software.

15. An apparatus for use in testing a digital system comprising a plurality of processors, the apparatus comprising:

a debugger;

a scheduler coupled to the debugger and operative to generate in response to signals from the debugger a set of debug commands for the processors;

at least one test command generator coupled to the scheduler and operative to generate test commands from the debug commands;

a chain manager coupled to the command generator and operative to define at least a subset of the processors as forming a group of processors to be subject to common control, to receive one or more of the test commands for each of the processors in the group, and to delay issuance of at least a subset of the test commands for the group until a designated group scan command is received for each of the processors in the group.

16. The apparatus of claim 15 further comprising a plurality of test command generators, with one of the test command generators associated with each of the processors.

17. The apparatus of claim 15 wherein one or more of the group scan commands for each of the processors in the group of processors are supplied by the chain manager as a single serial bit stream to a hardware scan chain associated with the processors.

18. The apparatus of claim 15 wherein the chain manager is implemented at least in part in software.

19. A method of testing a digital system comprising a plurality of processors, the method comprising the steps of:

defining at least a subset of the processors as forming a group of processors to be subject to common control;

receiving one or more commands for each of the processors in the group; and

delaying issuance of at least a subset of the commands for the group until a group scan command is received for each of the processors in the group.

20. An apparatus for use in testing a digital system comprising a plurality of processors, the apparatus comprising:

a chain manager operative to define at least a subset of the processors as forming a group of processors to be subject to common control, to receive one or more commands for each of

the processors in the group, and to delay issuance of the commands for the group until a designated group scan command is received for each of the processors in the group.